IN THE CLAIMS:

Please amend the claims as follows:

1. (Allowed) A single-chip integrated circuit for controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

memory, including one or more memory arrays for storing information related to the transceiver;

analog to digital conversion circuitry for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory;

an interface for allowing a host to read directly from and write directly to locations within the memory; and

comparison logic for comparing the digital values with limit values to generate flag values, wherein the flag values are stored in predefined locations within the memory during operation of the optoelectronic transceiver.

2. (Allowed) The single-chip integrated circuit of claim 1, further including:

a cumulative clock for generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable via the interface.

3. (Allowed) The single-chip integrated circuit of claim 1, further including:

a cumulative clock for generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is stored comprises one of the memory arrays of the memory.

4. (Allowed) The single-chip integrated circuit of claim 1, further including:

a power supply voltage sensor coupled to the analog to digital conversion circuitry, the power supply voltage sensor generating a power level signal corresponding to a power supply

voltage level of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory.

5. (Allowed) The single-chip integrated circuit of claim 4, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

6. (Allowed) The single-chip integrated circuit of claim 5, wherein

the comparison logic includes logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory; and

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

7. (Allowed) The single-chip integrated circuit of claim 4, wherein

the comparison logic includes logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

8. (Allowed) The single-chip integrated circuit of claim 1, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal

into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

9. (Allowed) The single-chip integrated circuit of claim 8, wherein

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

10. (Allowed) The single-chip integrated circuit of claim 1, further including

fault handling logic, coupled to the transceiver for receiving at least one fault signal from the transceiver, coupled to the memory to receive at least one flag value stored in the memory, and coupled to a host interface to transmit a computed fault signal, the fault handling logic including computational logic for logically combining the at least one fault signal received from the transceiver and the at least one flag value received from the memory to generate the computed fault signal.

E 1 cont

11. (Allowed) The single-chip integrated circuit of claim 1, further including

control adjustment circuitry for adjusting a first control signal of the control signals generated by the control circuitry in accordance with an adjustment value stored in the memory.

12. (Allowed) The single-chip integrated circuit of claim 1, wherein the control circuitry generates the first control signal in accordance with a temperature.

13. (Allowed) The single-chip integrated circuit of claim 1, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

14. (Allowed) A single-chip integrated circuit for monitoring an optoelectronic device, comprising:

memory, including one or more memory arrays for storing information related to the optoelectronic device;

analog to digital conversion circuitry for receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

a memory interface for allowing a host to read directly from and write directly to locations within the memory in accordance with commands received from a host device;

a power supply voltage sensor coupled to the analog to digital conversion circuitry, the power supply voltage sensor generating a power level signal corresponding to a power supply voltage level of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory; and

comparison logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

15. (Allowed) The single-chip integrated circuit of claim 14, further including:

a cumulative clock for generating a time value corresponding to cumulative operation time of the optoelectronic device, wherein the generated time value is readable via the memory interface.

16. (Allowed) The single-chip integrated circuit of claim 14, further including:

a cumulative clock for generating and storing in a register a time value corresponding to cumulative operation time of the optoelectronic device, wherein the register in which the time value is stored comprises one of the memory arrays of the memory.

17-18. Cancelled

17.
~~19.~~ (Allowed) The single-chip integrated circuit of claim 14, further including

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

18.
~~20.~~ (Allowed) The single-chip integrated circuit of claim 17, ~~19~~, wherein

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

Entry

21-22. Cancelled

19.
~~23.~~ (Allowed) The single-chip integrated circuit of claim 14, further including

fault handling logic, coupled to the optoelectronic device for receiving at least one fault signal from the optoelectronic device, coupled to the memory to receive at least one flag value stored in the memory, and coupled to a host interface to transmit a computed fault signal, the fault handling logic including computational logic for logically combining the at least one fault signal received from the optoelectronic device and the at least one flag value received from the memory to generate the computed fault signal.

20.
~~24.~~ (Allowed) The single-chip integrated circuit of claim 14, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

21.
~~25.~~ (Allowed) A single-chip integrated circuit for controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

analog to digital conversion circuitry for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital

values, and storing the digital values in predefined memory mapped locations within the integrated circuit;

comparison logic for comparing the digital values with limit values to generate flag values, wherein the flag values are stored in predefined memory mapped locations within the integrated circuit during operation of the optoelectronic transceiver;

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the integrated circuit; and

a memory mapped interface for allowing a host to read directly from and write directly to locations within the integrated circuit and for accessing memory mapped locations within the integrated circuit for controlling operation of the control circuitry.

22.
~~26.~~ (Allowed) A method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

in accordance with instructions received from a host device, enabling the host device to read directly from and write directly to locations within a memory; and

receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined locations within the memory during operation of the optoelectronic transceiver;

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory.

23.
~~27.~~ (Allowed) The method of claim 22 ~~26~~, further including:

generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable by the host device via a memory interface.

24.
~~28.~~ (Allowed) The method of claim 22 ~~26~~, further including:

generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is accessed by the reading step as a location in the memory.

25.
~~29~~. (Allowed) The method of claim ~~26~~ 22, further including:

converting an analog power supply voltage level signal, corresponding to a voltage level of the transceiver, into a digital power level value and storing the digital power level value in a predefined power level location within the memory.

26.
~~30~~. (Allowed) The method of claim ~~29~~ 25, further including:

generating a temperature signal corresponding to a temperature of the transceiver, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

27.
~~31~~. (Allowed) The method of claim ~~30~~ 26, including

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory; and

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

28.
~~32~~. (Allowed) The method integrated circuit of claim ~~29~~ 25, including

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

29. 22
~~33.~~ (Allowed) The method of claim ~~26~~, further including:

generating a temperature signal corresponding to a temperature of the transceiver, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

30. 29
~~34.~~ (Allowed) The method of claim ~~33~~, including:

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

31. 22
~~35.~~ (Allowed) The method of ~~26~~, further including

receiving at least one fault signal from the transceiver, receiving at least one flag value stored in the memory, logically combining the at least one fault signal received from the transceiver and the at least one flag value received from the memory to generate a computed fault signal, and transmitting the computed fault signal to the host device.

32. 22
~~36.~~ (Allowed) The method of claim ~~26~~, further including

adjusting a first control signal of the control signals in accordance with an adjustment value stored in the memory.

33. 22
~~37.~~ (Allowed) The method of claim ~~26~~, wherein the method is performed by a single-chip controller integrated circuit.

34. 22
~~38.~~ (Allowed) The method of claim ~~26~~, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

35.
~~39.~~ (Allowed) A method of monitoring an optoelectronic device, comprising:

in accordance with instructions received from a host device, enabling the host device to read directly from and write directly to locations within a memory;

receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

generating a power level signal corresponding to a power supply voltage level of the optoelectronic device, converting the power level signal into a digital power level value and storing the digital power level value in a predefined power level location within the memory; and

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory;

wherein the method is performed by a single-chip controller integrated circuit.

36. 48. (Allowed) The method of claim 35 ~~39~~, further including:

generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable by the host device via the memory interface.

37. ~~41~~. (Allowed) The method of claim 35 ~~39~~, further including:

generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is accessed by the reading step as a location in the memory.

42-43. Cancelled

38. ~~44~~. (Allowed) The method of claim 35 ~~39~~, further including

generating a temperature signal corresponding to a temperature of the optoelectronic device, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

39.
~~45.~~ (Allowed) The method of claim ~~44~~ 38, wherein

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

46-47. Cancelled

40.
~~48.~~ (Allowed) The method of claim ~~39~~ 35, further including

receiving at least one fault signal from the optoelectronic device, receiving at least one flag value stored in the memory, logically combining the at least one fault signal received from the optoelectronic device and the at least one flag value received from the memory to generate a computed fault signal, and transmit the computed fault signal to the host device.

41.
~~49.~~ (Allowed) The method of claim ~~39~~ 35, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

42.
~~50.~~ (Allowed) A method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

in accordance with instructions received from a host device, enabling the host device to read directly from and write directly to locations within a controller of the optoelectronic transceiver;

receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined memory mapped locations within the controller;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined memory mapped locations within the controller during operation of the optoelectronic transceiver; and

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in the predefined memory mapped locations within the controller.

43. 42
51. The method of claim 50, further including:

generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is accessed by the reading step as a memory mapped within the controller.

52-64. Cancelled

44.
65. (Allowed) A single-chip integrated circuit for monitoring an optoelectronic device, comprising;

memory, including one or more memory arrays for storing information related to the optoelectronic device;

E 1 cont

analog to digital conversion circuitry for receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signal into digital values, and storing the digital values in predefined locations within the memory;

a memory interface for allowing a host to read directly from and write directly to locations within the memory in accordance with commands received from a host device;

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory; and

comparison logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

45.
66. (Allowed) A method of monitoring an optoelectronic device, comprising;

in accordance with instructio ns received from a host device, enabling the host device to read directly from and write directly to locations within memory;

receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

generating a temperature signal corresponding to a temperature of the optoelectronic device, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory; and

comparing the temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory;

wherein the method is performed by a signal-chip controller integrated circuit.

Please add the following new claims:

46. (New) Circuitry for monitoring an optoelectronic device, comprising:

memory, including one or more memory arrays for storing information related to the optoelectronic device;

analog to digital conversion circuitry configured to receive a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, convert the received analog signals into digital values, and store the digital values in predefined locations within the memory;

comparison logic configured to compare the digital values with limit values to generate flag values, wherein the flag values are stored in predefined flag storage locations within the memory during operation of the optoelectronic device; and

an interface configured to enable a host to read from host-specified locations within the memory, including the predefined flag storage locations, in accordance with commands received from the host.

47. (New) The circuitry of claim 46, wherein the analog to digital conversion circuitry is configured to convert a power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory.

48. 46
~~69.~~ (New) The circuitry of claim ~~67~~, wherein the comparison logic includes logic for comparing the digital power level value with a power limit value, generating a power flag value based on the comparison of the digital power signal with the power limit value, and storing the power flag value in a predefined power flag location within the memory.

49. 46
~~70.~~ (New) The circuitry of claim ~~67~~, wherein the analog to digital conversion circuitry is configured to convert a temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

50. 49
~~71.~~ (New) The circuitry of claim ~~70~~, wherein the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

51. 46
~~72.~~ (New) The circuitry of claim ~~67~~, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

52. 46
~~73.~~ (New) The circuitry of claim ~~67~~, wherein the analog to digital conversion circuitry is configured to receive a voltage signal from a source external to the monitoring circuitry, convert the voltage signal into a digital voltage value and store the digital voltage value in a respective predefined location within the memory.

53.
~~74.~~ (New) Circuitry for monitoring an optoelectronic device, comprising:

memory, including one or more memory arrays for storing information related to the optoelectronic device;

analog to digital conversion circuitry configured to receive a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, convert the received analog signals into digital values, and store the digital values in predefined locations within the memory;

comparison logic configured to compare the digital values with limit values to generate flag values, wherein the flag values are stored in predefined flag storage locations within the memory during operation of the optoelectronic device; and

an interface configured to enable a host to read from host-specified locations within the memory, including the predefined flag storage locations, in accordance with commands received from the host;

wherein the plurality of analog signals include laser bias current, laser output power, and received power.

54.
75. (New) A method of monitoring an optoelectronic device, comprising:

receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined locations within a memory;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined flag locations within the memory; and

in accordance with instructions received from a host device, enabling the host device to read from host-specified locations within the memory, including the predefined flag locations.

55.
76. (New) The method of claim 54 75, further including:

generating a power level signal corresponding to a power supply voltage level of the optoelectronic device, converting the power level signal into a digital power level value and storing the digital power level value in a predefined power level location within the memory.

56.
77. (New) The method of claim 55 76, further including:

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

57.
78. (New) The method of claim 54 75, further including

generating a temperature signal corresponding to a temperature of the optoelectronic device, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

58. 79. (New) The method of claim 57 78, wherein

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

59. 80. (New) The method of claim 54 75, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

60. 81. (New) The method of claim 54 75, including receiving a voltage signal from a source external to the optoelectronic device, converting the voltage signal into a digital voltage value and storing the digital voltage value in a respective predefined location within the memory.

61. 82. (New) A method of monitoring an optoelectronic device, comprising:

receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined locations within a memory;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined flag locations within the memory; and

in accordance with instructions received from a host device, enabling the host device to read from host-specified locations within the memory, including the predefined flag locations;

wherein the plurality of analog signals includes laser bias current, laser output power, and received power.

62.
~~83.~~ (New) Circuitry for monitoring an optoelectronic device, comprising:

analog to digital conversion circuitry configured to receive a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, convert the received analog signals into digital values, and store the digital values in predefined memory-mapped locations within the optoelectronic device;

comparison logic configured to compare the digital values with limit values to generate flag values, wherein the flag values are stored in predefined memory-mapped flag storage locations within the optoelectronic device during operation of the optoelectronic device; and

an interface configured to enable a host to read from host-specified memory-mapped locations within the optoelectronic device, including the predefined memory-mapped flag storage locations.

63, 62
~~84.~~ (New) The circuitry of claim ~~83~~, wherein the analog to digital conversion circuitry is configured to convert a power level signal into a digital power level value and to store the digital power level value in a predefined memory-mapped power level location within the optoelectronic device.

64. 63
~~85.~~ (New) The circuitry of claim ~~84~~, wherein the comparison logic includes logic for comparing the digital power level value with a power limit value, generating a power flag value based on the comparison of the digital power signal with the power limit value, and storing the power flag value in a predefined memory-mapped power flag location within the optoelectronic device.

65. 62
~~86.~~ (New) The circuitry of claim ~~85~~, wherein the analog to digital conversion circuitry is configured to convert a temperature signal into a digital temperature value and to store the digital temperature value in a predefined memory-mapped temperature location within the optoelectronic device.

66. 65
~~87.~~ (New) The circuitry of claim ~~86~~, wherein the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit

value, and storing the temperature flag value in a predefined memory-mapped temperature flag location within the optoelectronic device.

67.
~~88.~~ (New) The circuitry of claim ~~83~~ 62, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

68.
~~89.~~ (New) The circuitry of claim ~~83~~ 62, wherein the analog to digital conversion circuitry is configured to receive a voltage signal from a source external to the monitoring circuitry, convert the voltage signal into a digital voltage value and store the digital voltage value in a respective predefined memory-mapped location within the optoelectronic device.

69.
~~90.~~ (New) Circuitry for monitoring an optoelectronic device, comprising:

analog to digital conversion circuitry configured to receive a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, convert the received analog signals into digital values, and store the digital values in predefined memory-mapped locations within the optoelectronic device;

comparison logic configured to compare the digital values with limit values to generate flag values, wherein the flag values are stored in predefined memory-mapped flag storage locations within the optoelectronic device during operation of the optoelectronic device; and

an interface configured to enable a host to read from host-specified memory-mapped locations within the optoelectronic device, including the predefined memory-mapped flag storage locations, in accordance with commands received from the host;

wherein the plurality of analog signals include laser bias current, laser output power, and received power.

70.
~~91.~~ (New) A method of monitoring an optoelectronic device, comprising:

receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined memory-mapped locations within the optoelectronic device;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined memory-mapped flag locations within the optoelectronic device; and

in accordance with instructions received from a host device, enabling the host device to read from host-specified memory-mapped locations within the optoelectronic device, including the predefined memory-mapped flag locations.

71.
~~92.~~ (New) The method of claim ~~91~~ 70, further including:

generating a power level signal corresponding to a power supply voltage level of the optoelectronic device, converting the power level signal into a digital power level value and storing the digital power level value in a predefined memory-mapped power level location within the optoelectronic device.

72.
~~93.~~ (New) The method of claim ~~92~~ 71, further including:

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined memory-mapped power level flag location within the optoelectronic device.

73.
~~94.~~ (New) The method of claim ~~91~~ 70, further including

generating a temperature signal corresponding to a temperature of the optoelectronic device, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined memory-mapped temperature location within the optoelectronic device.

74.
~~95.~~ (New) The method of claim ~~94~~ 73, wherein

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined memory-mapped temperature flag location within the optoelectronic device.

75. 70
~~96~~. (New) The method of claim ~~91~~, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

76. 70
~~97~~. The method of claim ~~91~~, including receiving a voltage signal from a source external to the optoelectronic device, converting the voltage signal into a digital voltage value and storing the digital voltage value in a respective predefined memory-mapped location within the optoelectronic device.

77.
~~98~~. (New) A method of monitoring an optoelectronic device, comprising:

receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined memory-mapped locations within the optoelectronic device;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined memory-mapped flag locations within the optoelectronic device; and

in accordance with instructions received from a host device, enabling the host device to read from host-specified memory-mapped locations within the optoelectronic device, including the predefined memory-mapped flag locations;

wherein the plurality of analog signals includes laser bias current, laser output power, and received power.

E1 cont.